The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A ~~limiter comprising:~~ semiconductor device comprising a limiter,

wherein the limiter includes:

a transistor including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate is formed over the semiconductor layer with a first insulating film interposed therebetween;

the floating gate and the control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal, [[and]]

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

2. (Currently Amended) A ~~limiter comprising:~~ semiconductor device comprising a limiter,

wherein the limiter includes:

a transistor including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate is formed over the semiconductor layer with a first insulating film interposed therebetween;

the floating gate and the control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

a source of the transistor is connected to an input terminal and an output terminal, [[and]]

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

3. (Currently Amended) A ~~limiter comprising:~~ semiconductor device comprising a limiter,

wherein the limiter includes:

a plurality of transistors each including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate of each of the plurality of transistors is formed over the semiconductor layer of each of the plurality of transistors with a first insulating film interposed therebetween;

the floating gate and the control gate of each of the plurality of transistors overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of each of the plurality of transistors is covered with a third insulating film;

a drain of each of the plurality of transistors is connected to the control gate of each of the plurality of transistors;

the plurality of transistors are connected in series so as to have the same forward current direction; and

the drain and the control gate of one of the plurality of transistors are connected to an input terminal and an output terminal, [[and]]

wherein the floating gate of each of the plurality of transistors is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

4. (Currently Amended) A ~~limiter comprising:~~ semiconductor device comprising a limiter,

wherein the limiter includes:

a plurality of transistors each including a semiconductor layer, a floating gate and a control gate,

wherein the floating gate of each of the plurality of transistors is formed over the semiconductor layer of each of the plurality of transistors with a first insulating film interposed therebetween;

the floating gate and the control gate of each of the plurality of transistors overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of each of the plurality of transistors is covered with a third insulating film;

a drain of each of the plurality of transistors is connected to the control gate of each of the plurality of transistors;

the plurality of transistors are connected in series so as to have the same forward current direction; and

a source of one of the plurality of transistors is connected to an input terminal and an output terminal, [[and]]

wherein the floating gate of each of the plurality of transistors is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

5. (Currently Amended) A ~~limiter comprising:~~ semiconductor device comprising a limiter,

wherein the limiter includes:

a first transistor, and

a second transistor,

wherein a floating gate of the first transistor is formed over a semiconductor layer of the first transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the first transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of the first transistor is covered with a third insulating film;

a drain of the first transistor is connected to the control gate of the first transistor;

a drain of the second transistor is connected to a gate of the second transistor;

the first transistor and the second transistor are connected in series so as to have the same forward current direction; and

the drain of the second transistor and the control gate are connected to an input terminal and an output terminal, [[and]]

wherein the floating gate of the first transistor is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

6. (Currently Amended) A ~~limiter comprising:~~ semiconductor device comprising a limiter,

wherein the limiter includes:

a first transistor, and

a second transistor,

wherein a floating gate of the first transistor is formed over a semiconductor layer of the first transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the first transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate of the first transistor is covered with a third insulating film;

a drain of the first transistor is connected to the control gate of the first transistor;

a drain of the second transistor is connected to a gate of the second transistor;

the first transistor and the second transistor are connected in series so as to have the same forward current direction; and

a source of the second transistor is connected to an input terminal and an output terminal, [[and]]

wherein the floating gate of the first transistor is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

7. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 1 further comprising a connecting terminal, wherein the connecting terminal is connected to the drain of the transistor.

8. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 1 further comprising a resistor, wherein the drain of the transistor is connected to the input terminal through the resistor.

9. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 1, wherein the transistor is a thin film transistor.

10. (Currently Amended) A semiconductor device comprising:

an integrated circuit, and

an antenna connected to the integrated circuit,

wherein the integrated circuit includes a limiter;

the limiter includes a transistor;

a floating gate of the transistor is formed over a semiconductor layer of the transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal, [[and]]

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change a limit voltage by controlling an amount of charge accumulated in the floating gate.

11. (Currently Amended) A semiconductor device comprising an integrated circuit and an antenna connected to the integrated circuit,

wherein the integrated circuit includes a limiter, a pulse generation circuit for controlling a limit voltage of the limiter, and a booster circuit for supplying a power supply voltage to the pulse generation circuit;

the limiter includes a transistor;

a floating gate of the transistor is formed over a semiconductor layer of the transistor with a first insulating film interposed therebetween;

the floating gate and a control gate of the transistor overlap each other with a second insulating film interposed therebetween;

a side surface of the floating gate is covered with a third insulating film;

a drain of the transistor is connected to the control gate; and

the drain and the control gate are connected to an input terminal and an output terminal; [[and]]

wherein the floating gate is electrically floating, and

wherein the limiter is configured to change the limit voltage by controlling an amount of charge accumulated in the floating gate.

12. (Original) The semiconductor device according to claim 10 or 11, wherein the transistor is a thin film transistor.

13. (Previously Presented) The semiconductor device according to claim 10 or 11 further comprising a resistor, wherein the drain of the transistor is connected to the input terminal through the resistor.

14. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 2 further comprising a connecting terminal, wherein the connecting terminal is connected to the source of the transistor.

15. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 3 further comprising a connecting terminal, wherein the connecting terminal is connected to the drain of the one of the plurality of transistors.

16. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 4 further comprising a connecting terminal, wherein the connecting terminal is connected to the source of the one of the plurality of transistors.

17. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 5 further comprising a connecting terminal, wherein the connecting terminal is connected to the drain of the second transistor.

18. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 6 further comprising a connecting terminal, wherein the connecting terminal is connected to the source of the second transistor.

19. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 2 further comprising a resistor, wherein the source of the transistor is connected to the input terminal through the resistor.

20. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 3 further comprising a resistor, wherein the drain of the one of the plurality of transistors is connected to the input terminal through the resistor.

21. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 4 further comprising a resistor, wherein the source of the one of the plurality of transistors is connected to the input terminal through the resistor.

22. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 5 further comprising a resistor, wherein the drain of the second transistor is connected to the input terminal through the resistor.

23. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 6 further comprising a resistor, wherein the source of the second transistor is connected to the input terminal through the resistor.

24. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 2, wherein the transistor is a thin film transistor.

25. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 3, wherein the plurality of transistors are thin film transistors.

26. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 4, wherein the plurality of transistors are thin film transistors.

27. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 5, wherein the second transistor is a thin film transistor.

28. (Currently Amended) The ~~limiter~~ semiconductor device according to claim 6, wherein the second transistor is a thin film transistor.